



The very long LEON / NOEL story

Gaisler 25 Years In Space

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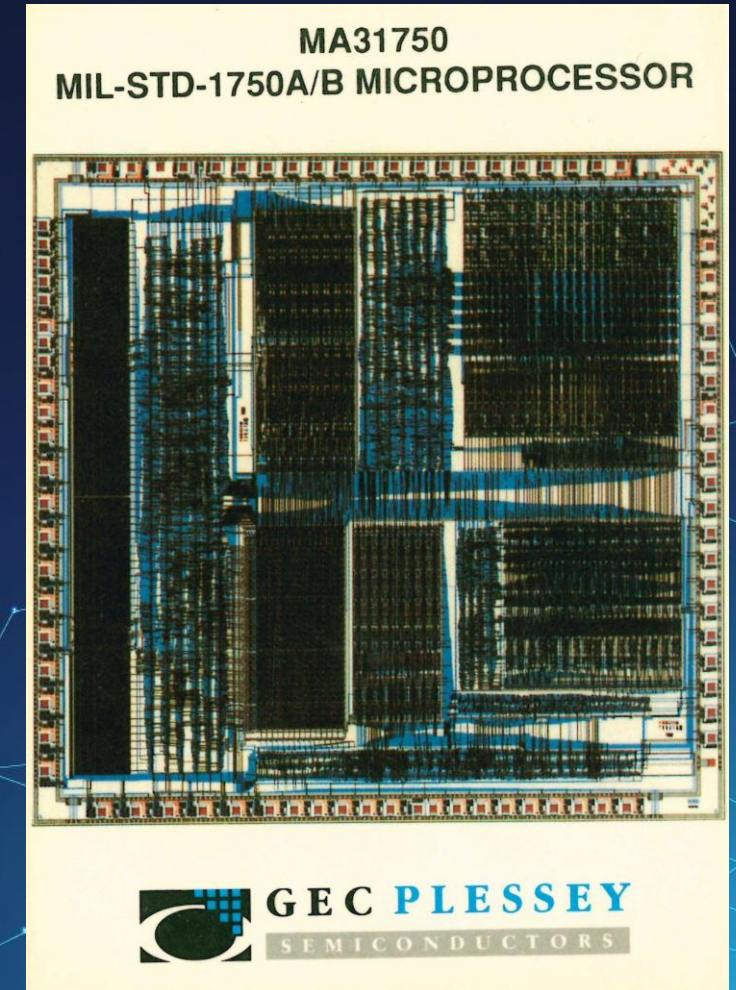
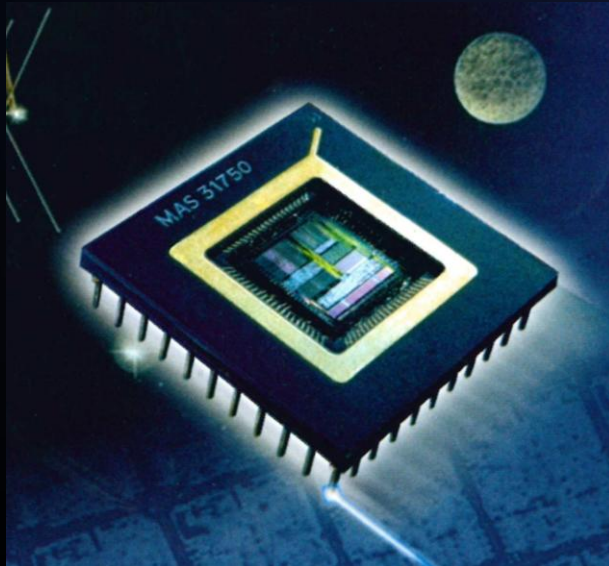
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→ THE EUROPEAN SPACE AGENCY

First steps in Europe – US IP – MIL-STD-1750A

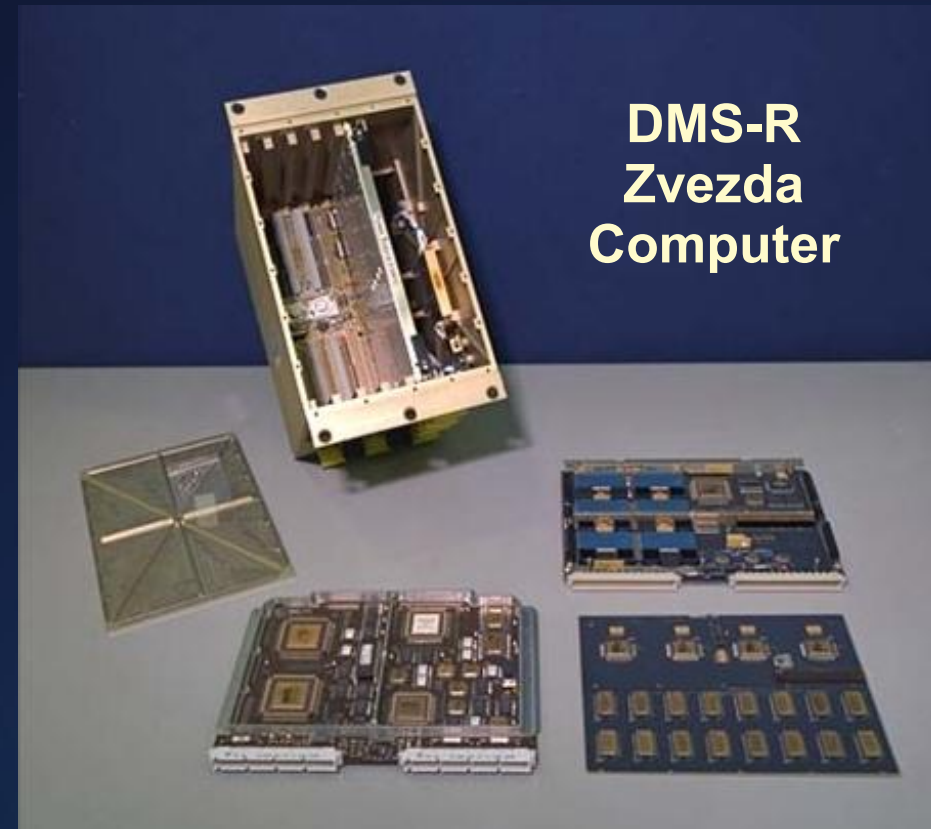
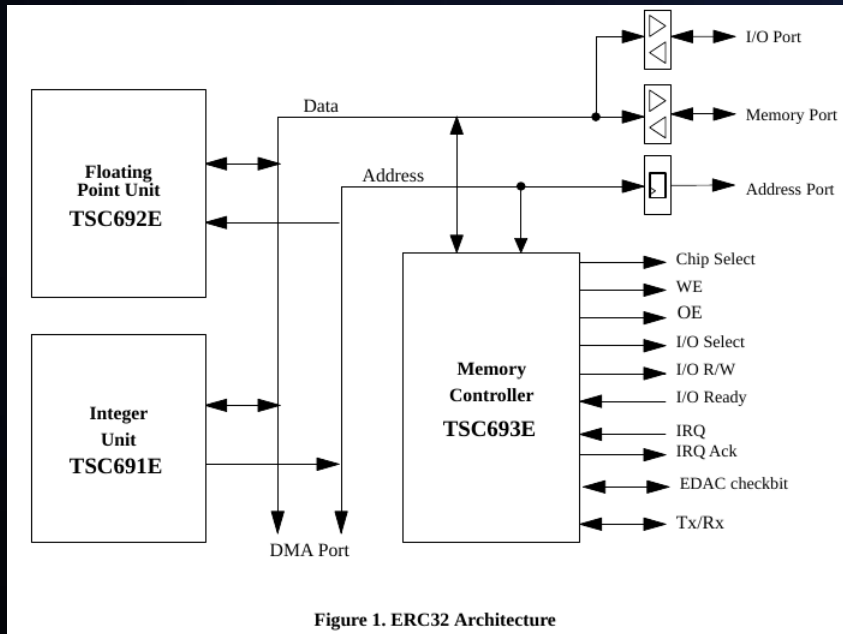
- MEDL (Marconi Electronic Devices Ltd) / Plessey / Dynex (Lincoln, UK) 1.5 μ m SOS, clone of MDC281
- Late 1980's : MS281 chipset
 - MA17501 Execution Unit (EU)
 - MA17502 Control Unit (CU)
 - MA17503 Interrupt Unit (IU)
- Begin 1990's : MA31750 single chip
- TO André Pouponnot



ERC32 : 1990s: Moving to SPARC open ISA

US IP (Cypress), European Fab: Temic/Atmel (now Microchip)
Chipset: 0.8 μm – steering the ISS
Single-chip : 0.5 μm – still on catalog
ESA TO's = future Gaisler people

SPARC



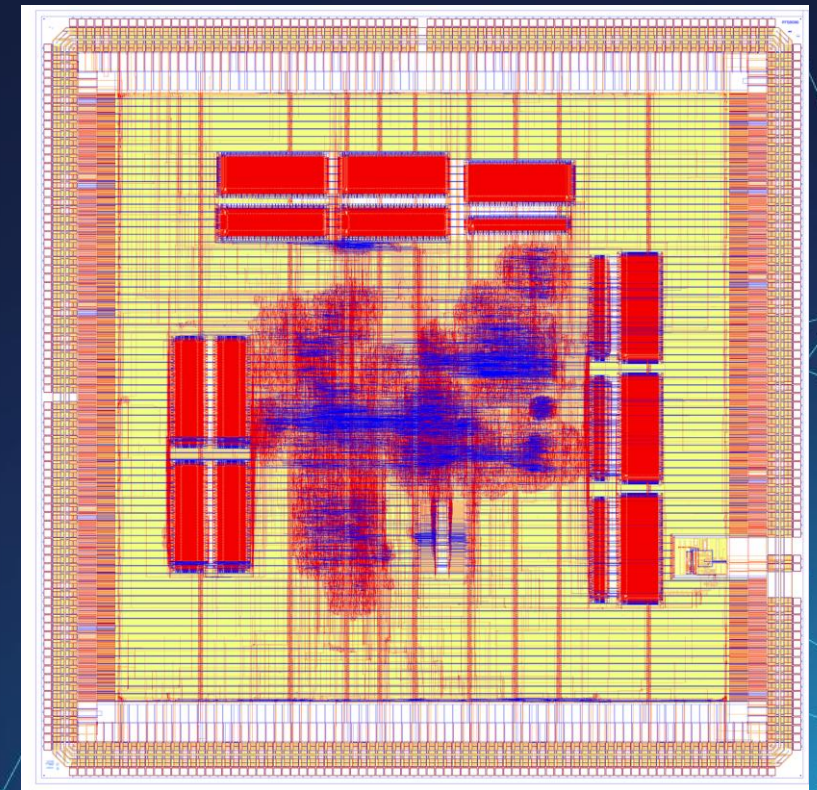
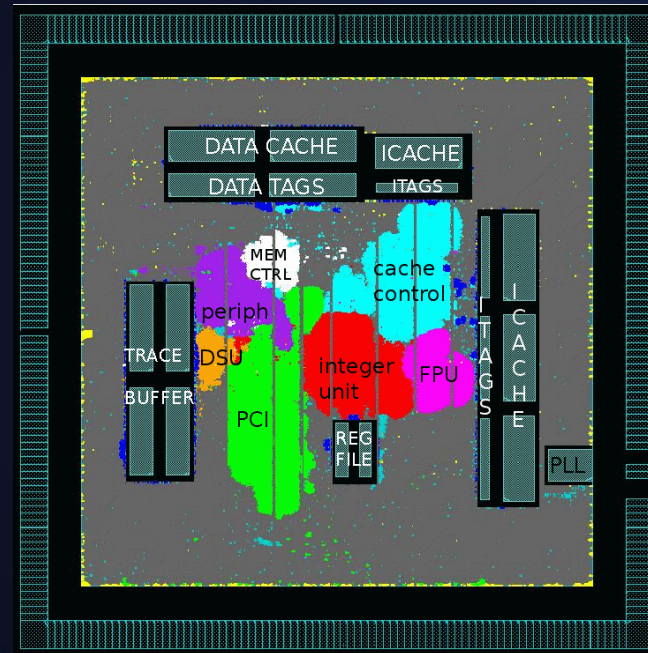
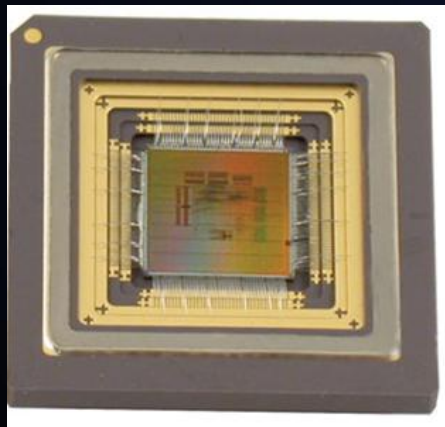
LEON2 : 2000's: moving to European IP

LEON2 SPARC V8 IP core, designed at ESA and Gaisler Research
AT697 single core 100 MHz, 180nm process (France, later UMC Taiwan)

Collaboration Atmel-ESA-Gaisler

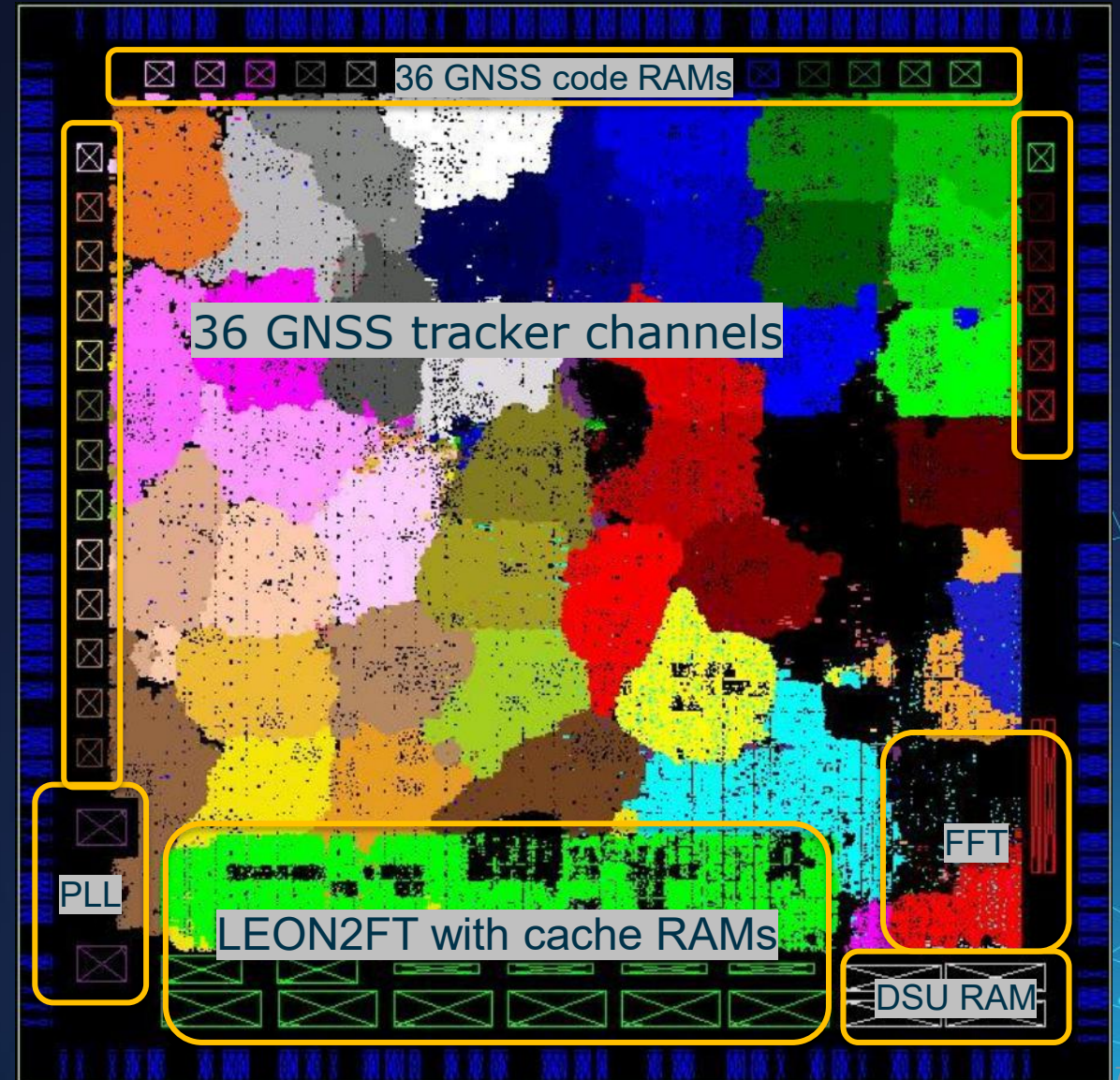
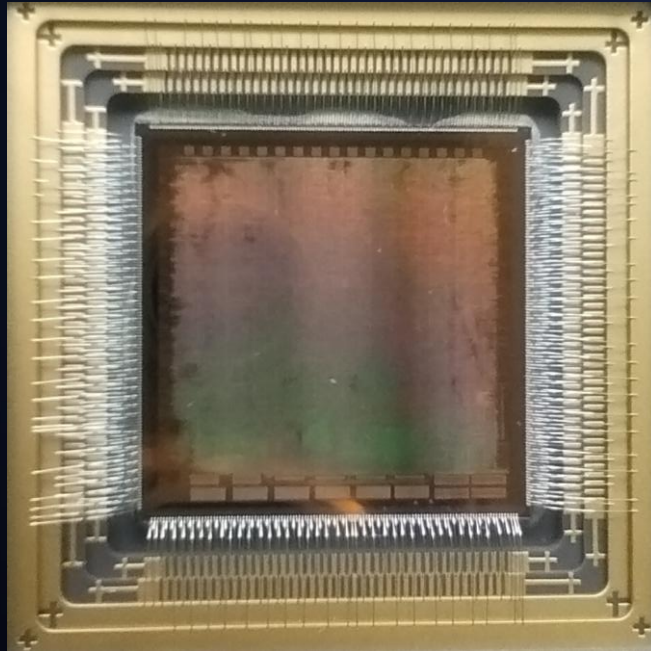
Intense hands-on support 😊

ESA TO André Pouponnot



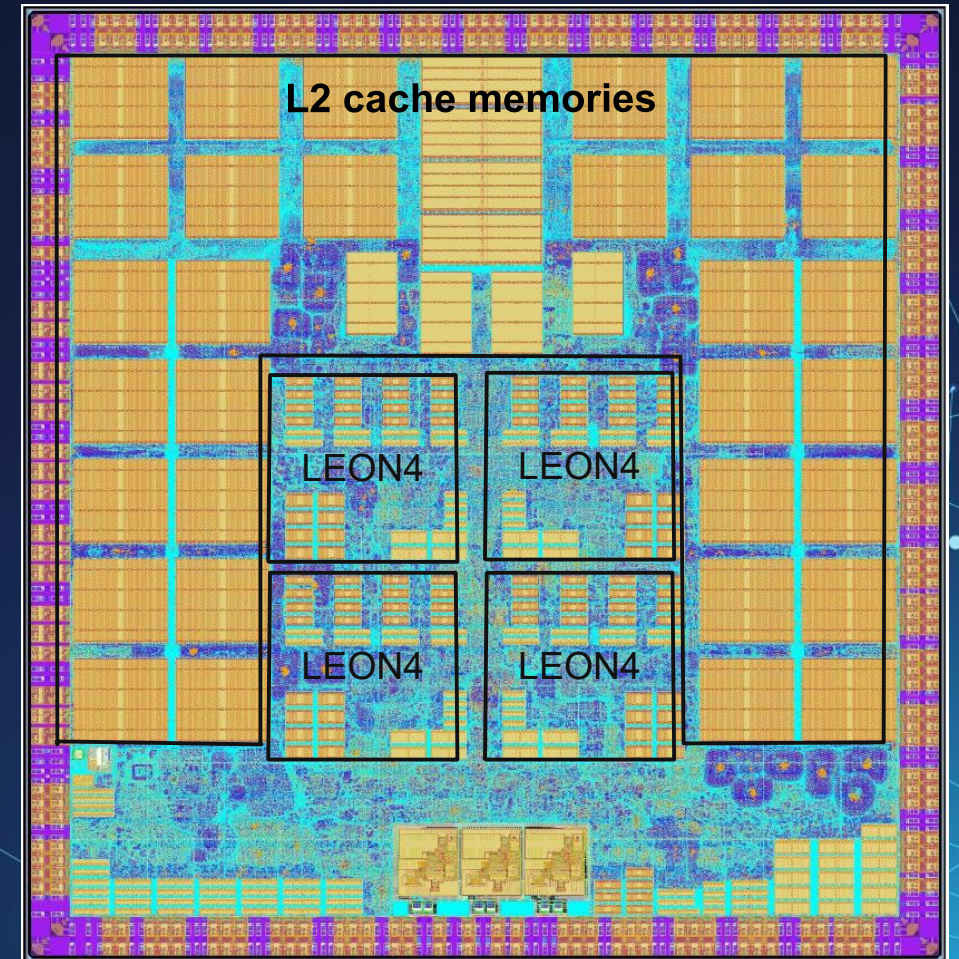
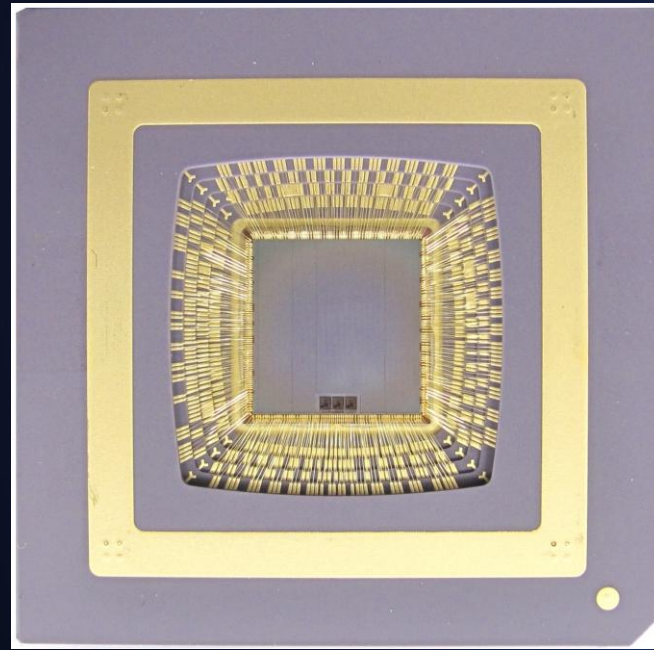
LEON2 spin-off ASICs : example AGGA4

- LEON2 and LEON3 used in many FPGA ASIC / ASSP
- AGGA4 = SoC LEON2 with GRFPU, SPW, 1553, ...
 - 36 GNSS baseband channels
 - Fab 2013 in Atmel 180nm
- Driven by Earth Observation
 - Radio-Occultation, Precise Orbit Determination
 - METOP-SG, Sentinel's and others
- TO P. Silvestrin
- TO J. Roselló
- Very intense hands-on 😊



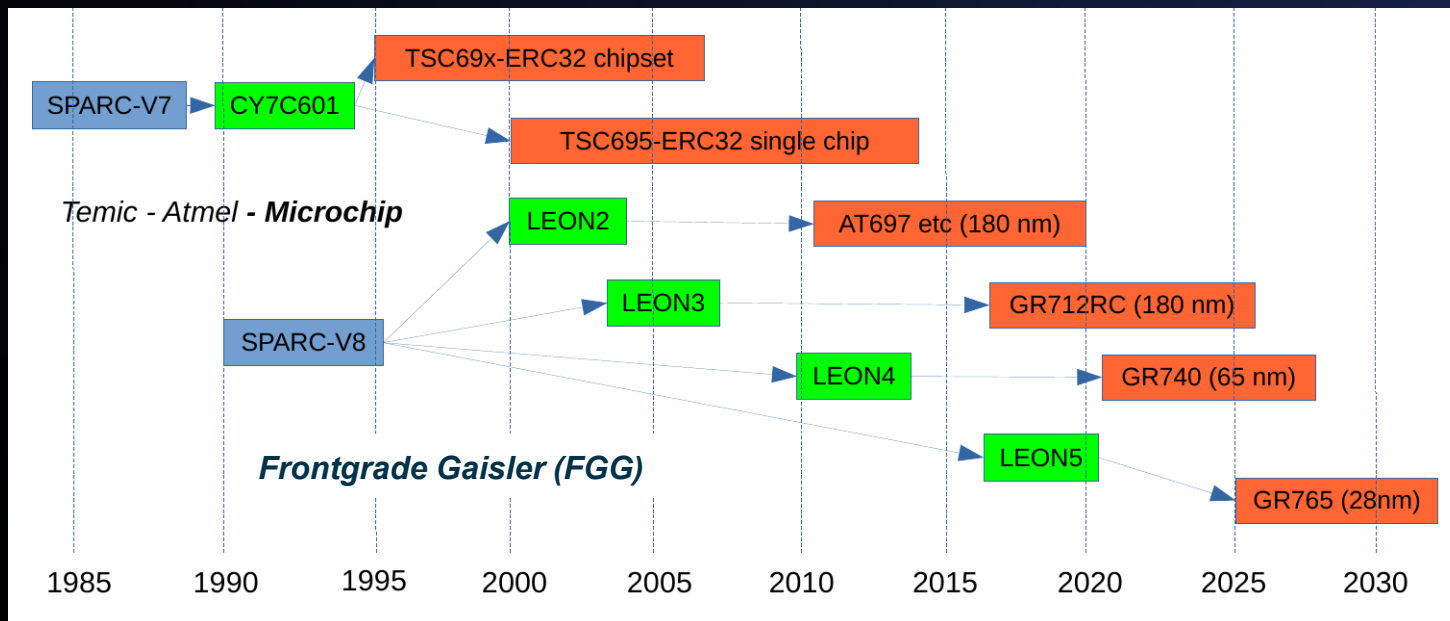
GR740 : 2010's: Multi-Core, European IP/design/foundry

- 4x LEON4 SPARC V8 IP core – first multi-core on ESA contract
- ST Microelectronics (France) 65nm process
- André Pouponnot retired in 2008
- Management - no more hands-on ☹️
- Successfully flying since 2024



SPARC in space > 25 years – 5 generations

- ERC32 – Based on a commercial SPARC-V7 IP-core, TSC69x series, 0.8 / 0.5 μm
- LEON2 SPARC V-8 IP-core owned by ESA → Atmel AT697F in 180nm
- LEON3 IP-core by Frontgrade Gaisler → GR712RC, 180 nm Ramon RH lib, Tower 180nm
- LEON4 IP-core, introducing L2 cache → GR740 in ST 65nm, QML-V in 2022
- LEON5, introducing dual-issue → GR765 started 2021 as upgrade to GR740, 65 → 28 nm
- Many other ASIC/FPGA with LEON2/3 IP (SCOC3, AGGA4, MDPA, RTC, COLE, BEPI, ...)



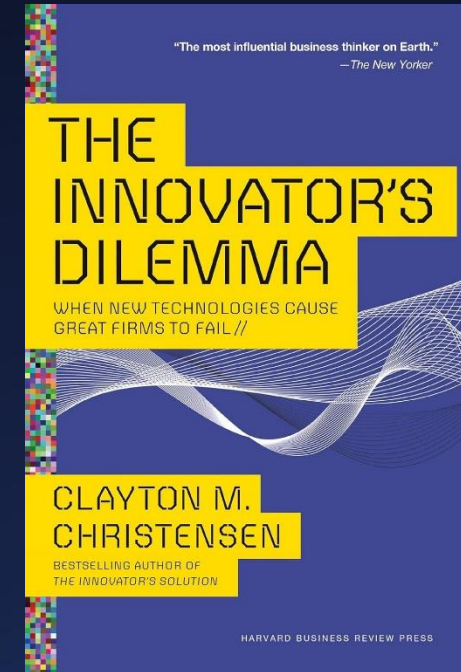
LEON in all ESA missions
Export to US, China, Japan, Korea
More than 20000 flight parts
SPARC used in India, Russia...

WHAT'S NEXT?

New challenges after SPARC

The Innovator's Dilemma (1997)

Disruptive innovation vs technology improvement
When new technologies cause great firms to fail

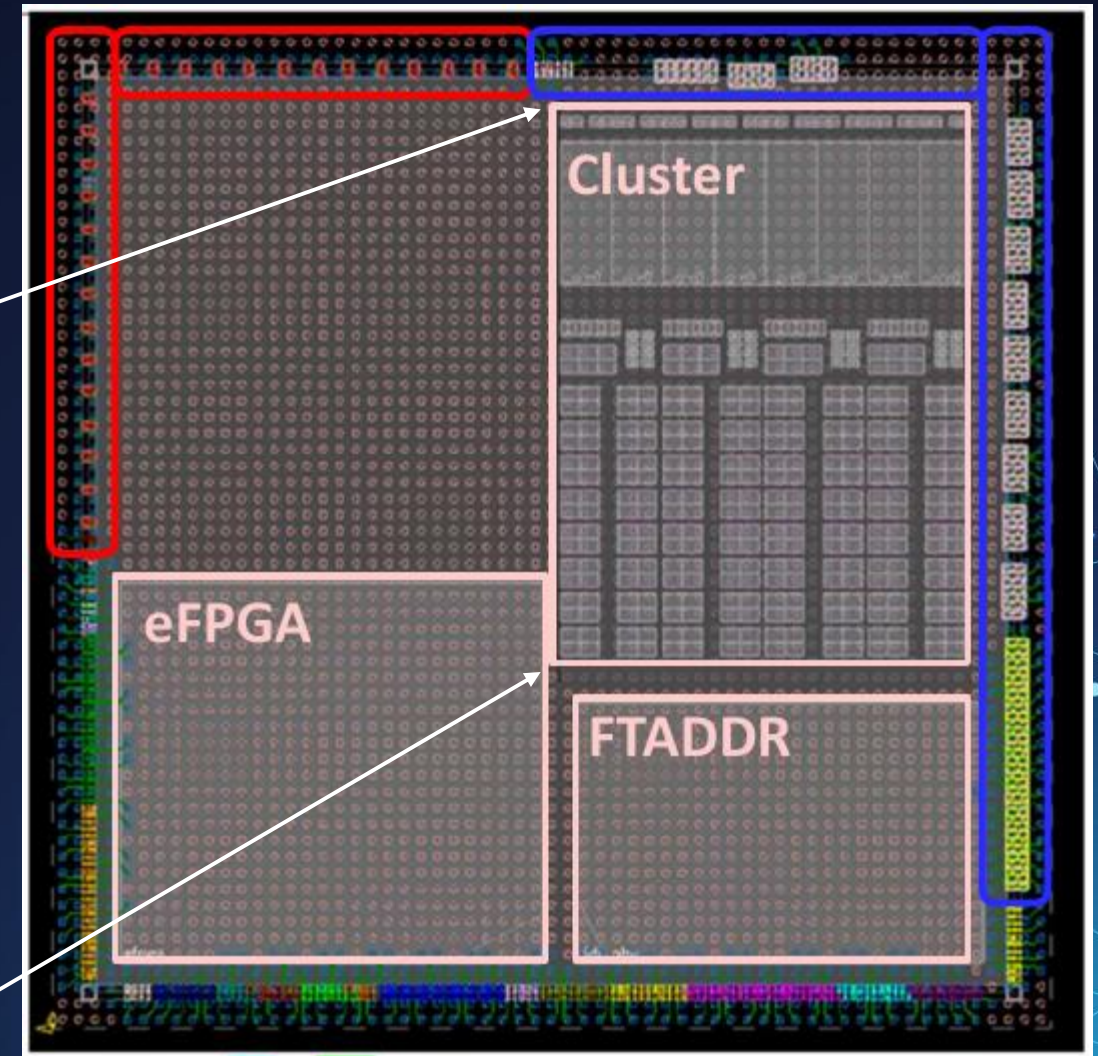
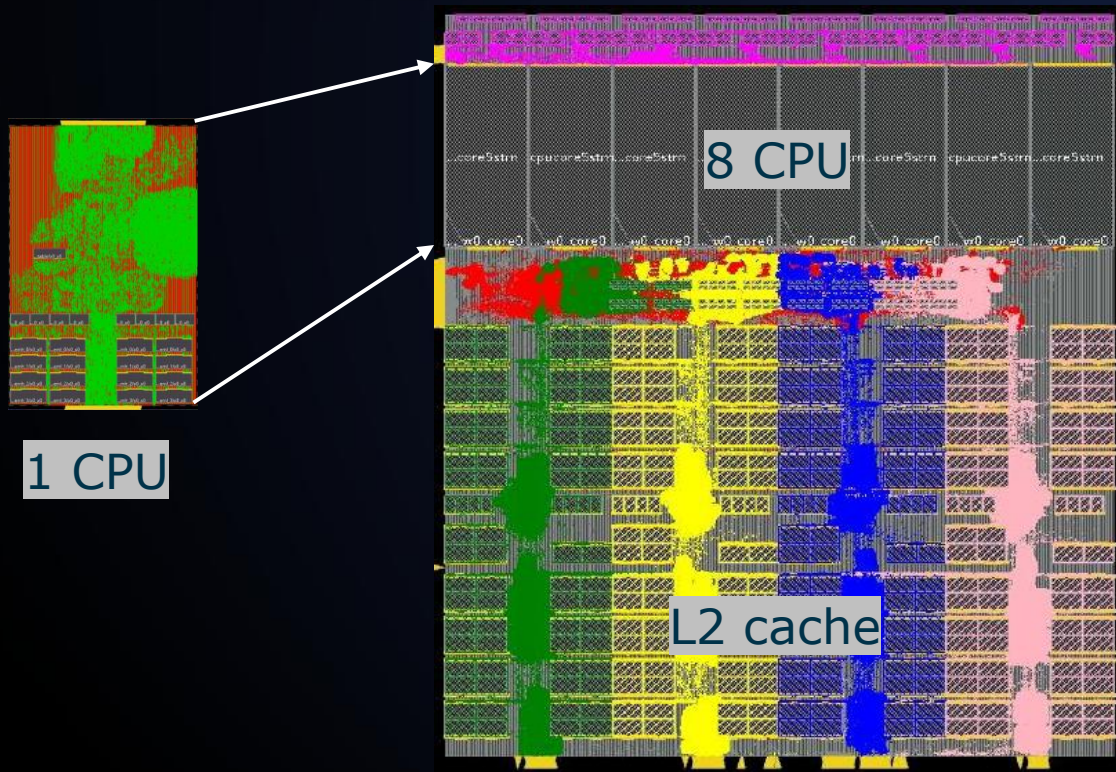


- SPARC is great – but becoming obsolete
 - No more young engineers from university
- 2015 : First talks about RISC-V at ESA
 - Little enthusiasm – two camps: SPARC / ARM
- 2018: Starting with small ESA studies (ITI, today = OSIP)
 - Gaisler internal NOEL-V IP development
- 2022: TDE “RV Microprocessor Prototype” (450k)
- 2024: RISC-V HW / SW Ecosystem (2 M€)
- 2026: GR765 ...



GR765 – Octacore (8xSPARC or 8xRISC-V)

- ISA transition: Same chip runs SPARC or RISC-V
- Technology scaling from 65 to 28nm ST
- Enhanced memory: DDR SDRAM
- Interfaces: SerDes (PCIe, Ethernet, SpFi)
- Flexibility / customisation: eFPGA

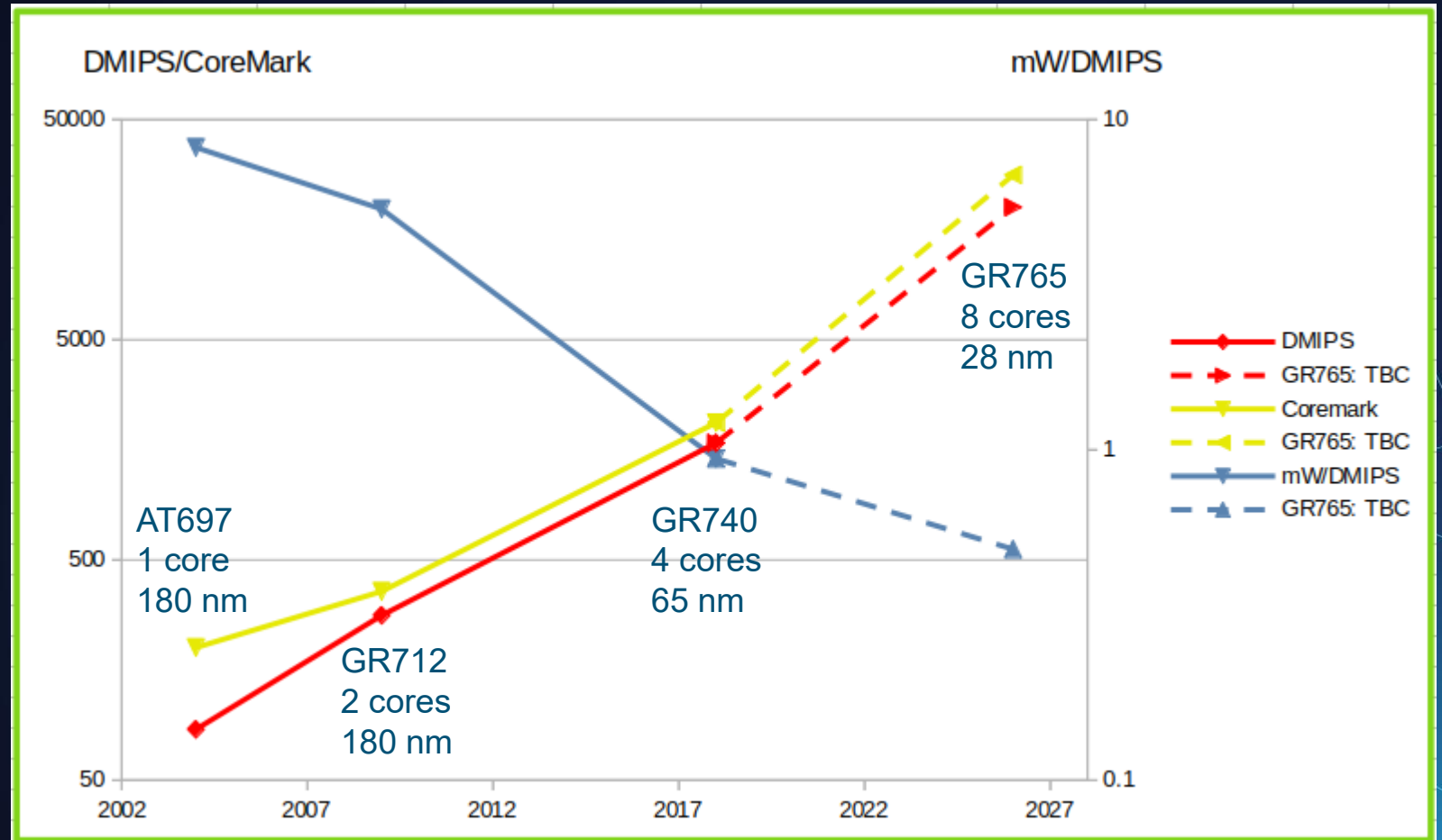


Achievements

- Transparent rad-hard
- Performance x10 / gen
- 1 generation / 8 years
- Power reduction

Future Challenges

- Increase performance
- **Massive** power reduction
- **Dhrystone/CoreMark**
- Parallel / AI workloads
- Reduced quantization
- Data volume & patterns
- IO (SerDes, D2D, PCIe)
- Cybersecurity
- Accelerate schedule



One processor generation every 8 years – isn't that slow?

- The score is not bad at all – compare with other public projects (IMF...?)
- Do not compare with commercial chip industry – space is a niche market with high NRE
 - We do fewer tape-outs, we skip technology nodes, but we make bigger leaps
 - In 8 years we get 10x performance, Moore's law is fulfilled: (2x transistors in 2 years)

How to get to 4x performance every 4 years?

- Mission creep : we engineers always want more, features, performance, ...
 - Learn to say no
- Overestimation of technology capabilities, and resources
 - Focus on key products: limit parallel developments
- Overheads in ESA R&D “top-down procurement” contracts
 - Public Funding requires accountability
 - Focus on outputs, products instead of micro-management
 - Move to “**Public-Private Partnership (PPP)**”



Keys for Gaisler's success

A team of excellent and highly motivated engineers

- Transparency : open ISA, open spec, open source, open bugs (“application notes”)
- Customer support: several IPN, but no ESA alert on Gaisler components
- Perseverance : don't give up even if it takes a bit longer
- Independence from equipment manufacturers
- Transatlantic setup : Aeroflex component expertise + Gaisler IP expertise
- Clean room approach : Products with predominantly European IP & supply chain
- Continuous effort on the Software Ecosystem
- Fundraising
 - ESA, Delegations, EC
 - Investors
- PR : conferences, sales, ads, events
→ yes, it's part of the business



Conclusion and Prospects

- Congratulations! – It has been a pleasure to work for 25 years with a team of **people who believe in what they are doing**
- Looking forward to work with you on the next generation
 - 16 cores, 7 nm, Vector, Accelerators, Security ... (GR7xV)
 - Power efficiency is a strong driver
- Leverage your background, maintain and improve IP
- Be open for disruptive new product ideas – AI, SNN
 - Seed the GRAINs for continued success
- Keep listening and supporting your customers
- Don't forget the software SDE
- Keep going! – **All the best for the next 25 years**

