



# Keeping Influencing the Architecture of Space Processors for the next 25 years

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# Introduction

- ⌘ BSC is a public research institution, established in 2005
- ⌘ Former CAOS (Computer Architecture / Operating Systems Interface) group, focused on computer architecture research on safety critical systems
- ⌘ Nowadays High Performance Embedded Systems (HPES) Laboratory
- ⌘ HArdware Dependability for Embedded Systems (HADES) Group
  - ⌘ strong focus on space systems

# BSC contributions to the Architecture of Space Processors

- ⌘ How it all started
- ⌘ 2010: Gaisler introduces the first prototype of NGMP (Next Generation Multiprocessor) based on LEON4 (SPARC v8)
- ⌘ ESA contract for the first evaluation of its multicore performance
- ⌘ Multicore microbenchmark technology
- ⌘ Generated up to 9x slowdown on the 4 core configuration [1]
- ⌘ Initial feedback helped to improve the NGMP design
- ⌘ Ever since a close partnership with Gaisler and ESA, providing feedback to space processor designs, including GR765



[1] M. Fernandez et al, Assessing the suitability of the NGMP multi-core processor in the space domain, EMSOFT 2012

# BSC contributions to the Architecture of Space Processors

- ❧ 2009-2015 PROARTIS and PROXIMA projects
- ❧ 2013-2014 PROARTIS4SPACE ESA project
- ❧ Lead by BSC, participation by Gaisler and major avionics/aerospace partners
- ❧ Increased the timing predictability of NGMP
  - ❧ Technology transfer of the hardware proposals of my PhD
- ❧ BSC obtained its own Vendor ID (0x0E) in Gaisler's GRLIB IP Core Library

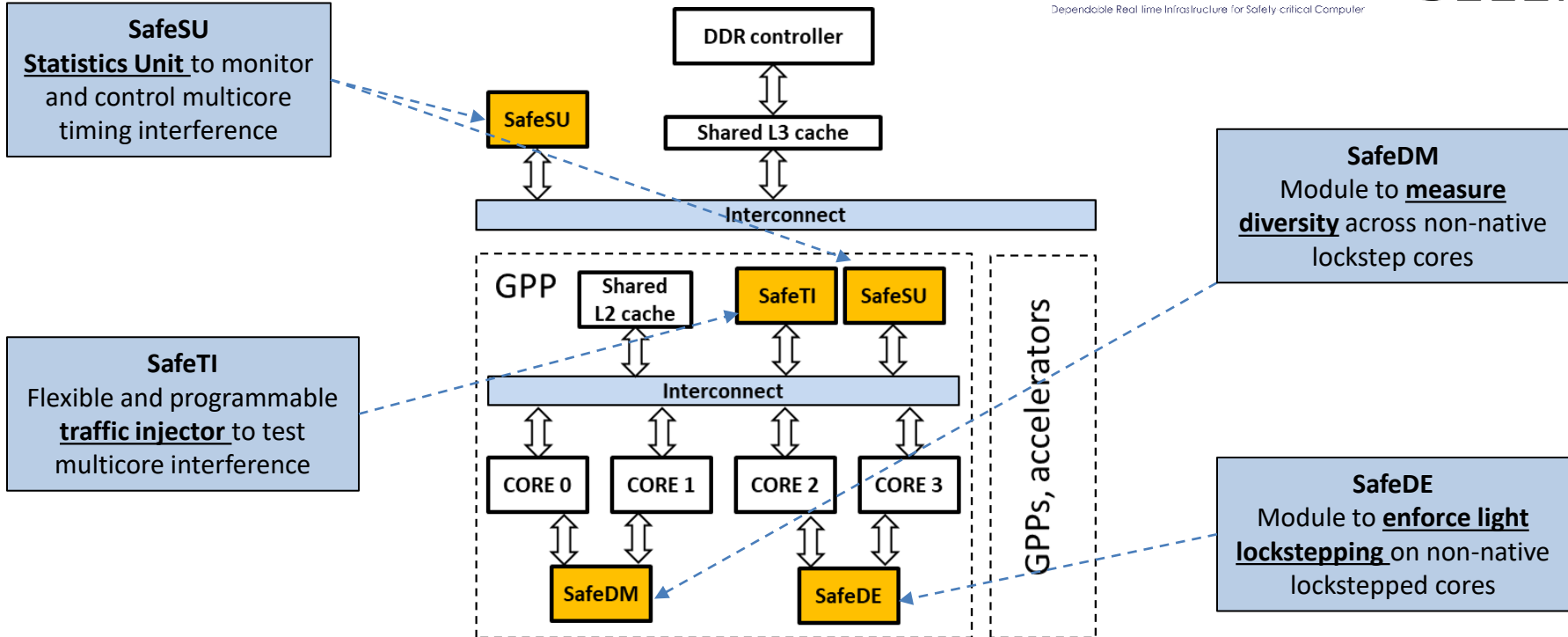


**PROXIMA**



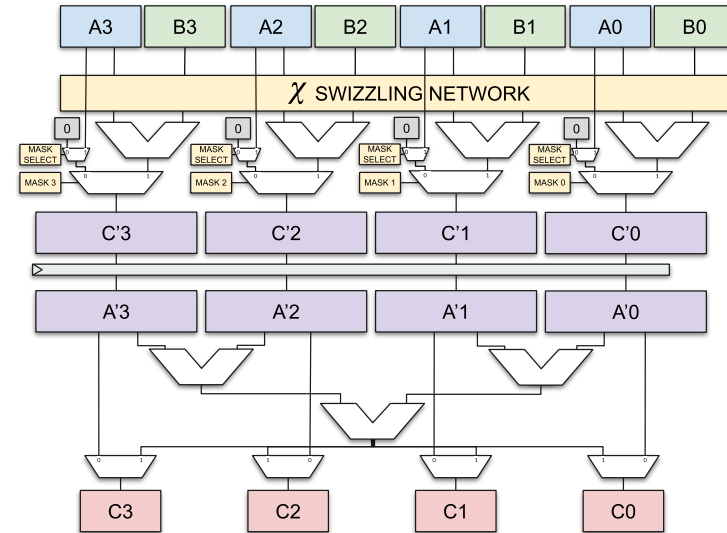
- ❧ Available from Gaisler for licensing: LEON3 Probabilistic Platform  
<https://www.gaisler.com/products/leon3>

# BSC and space processors design and evaluation

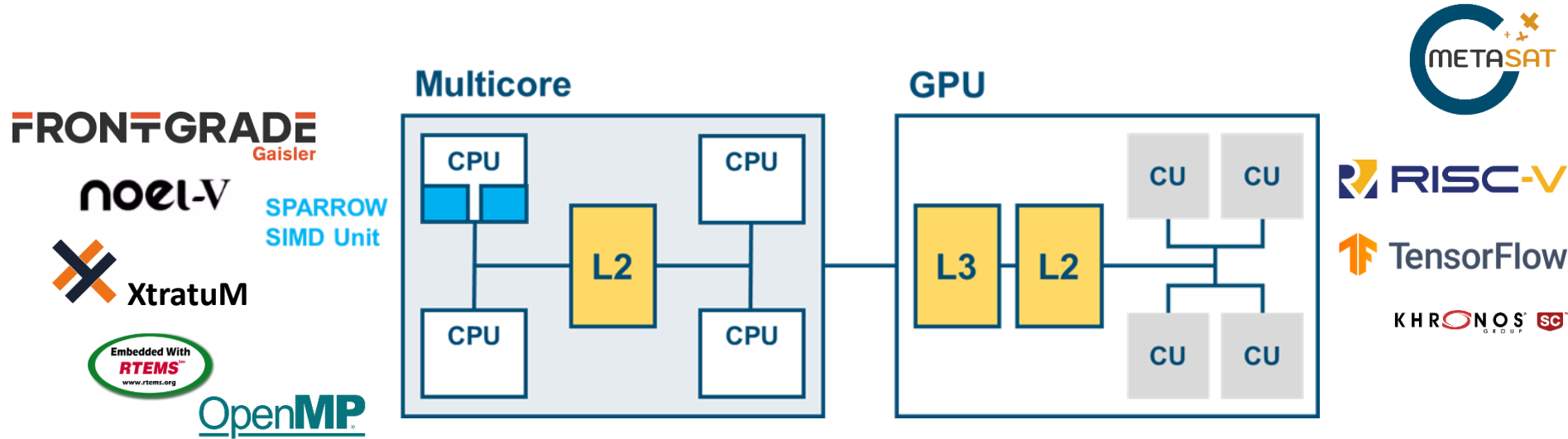


# SPARROW: Hw/Sw Co-designed SIMD Unit for AI acceleration

- ⌘ Increase the machine learning processing capabilities of space processors
- ⌘ Portable, open source design, integrated with NOEL-V (RISC-V) and LEON 3 (SPARC)
- ⌘ High-performance, Low-cost targeting both ASIC and FPGA implementations, at least 30% smaller than conventional vector processors with similar performance
- ⌘ Minimal core modifications → incremental qualification
- ⌘ Key features: reuse of integer register file, short SIMD unit (8-bit), swizzling, reductions



# The METASAT Heterogeneous Platform



- Qualifiable Software Stack: accelerators can be used from bare metal or RTEMS SMP
- Mixed-criticality: TSP support
- Added support in Model-based design tools
- Standard-based Digital Twin framework

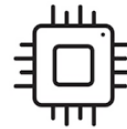


# The future

- ⌘ Increase the TRL of existing prototypes

- ⌘ Tape outs

- ⌘ Integration with other Gaisler cores (LEON5, NOEL3)



**LEON**  
**NOEL3**

- ⌘ Higher Performance:

- ⌘ General Purpose SIMD

- ⌘ Vector processing

- ⌘ Increase GPU performance



**RISC-V**

- ⌘ New features

- ⌘ Support official RISC-V extensions and influence their design



# The future

## Security

- Post Quantum Cryptography (PQC) acceleration
- Dedicated accelerators
- Custom Instructions



**SMARTY**

**PQC4eMRTD**

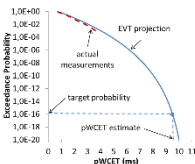
## Safety

- Timing predictability
- WCET support
- Multicore interference



# Don't forget about the software!

- Hardware doesn't have value without software
- Mature software stack further
- Frameworks to achieve higher productivity, performance, easier development, debugging and verification
- Operating system support and drivers for high accelerators
- Standardised Safety Critical Parallel programming APIs
- Full application demonstrators and benchmarks



# Conclusion

- ⌘ Long-term close R&D collaboration between BSC and Gaisler
- ⌘ Applied research with technology transfer
- ⌘ We will continue to advance together the architecture of future space processors

# Acknowledgements

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Thank you!

Questions?

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