

# Mission and computing

2026-02-05





Established 2001 as a spin-off from  
Chalmers and European Space Agency



Located in Gothenburg, Sweden  
80+ employees in Sweden, Germany,  
France, Spain, and United Kingdom



Experts in fault-tolerant computing



Single minded focus on one thing only –  
*radiation hardened microprocessors for space*





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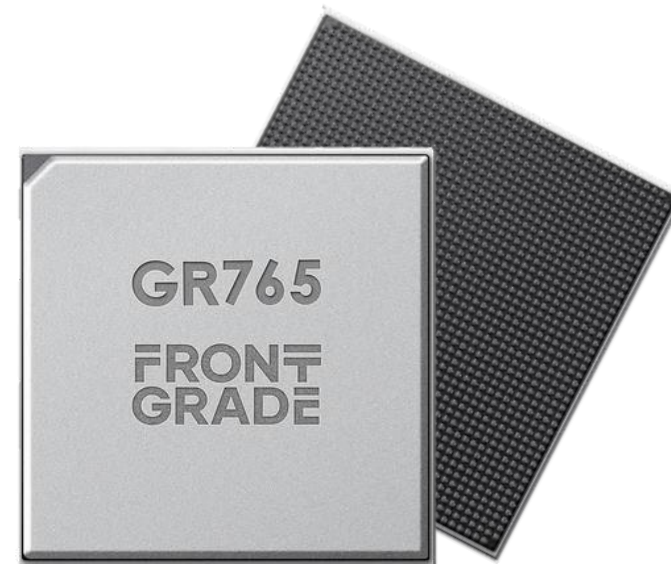
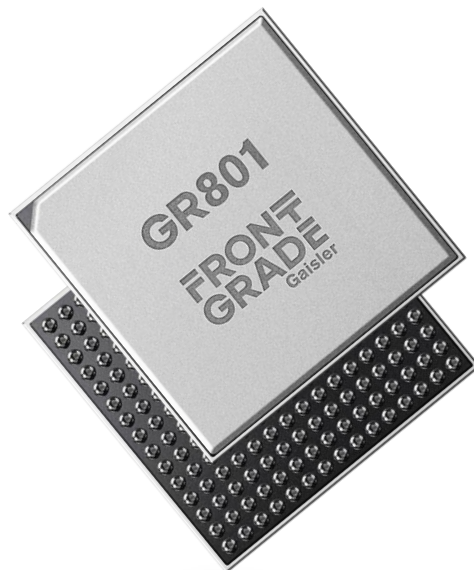
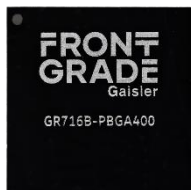
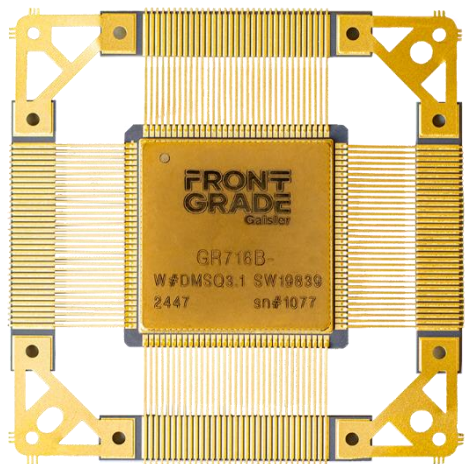
Experts in fault-tolerant computing



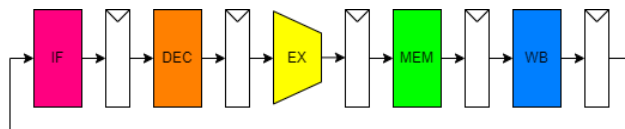
Single minded focus on one thing only –  
*radiation hardened microprocessors for space*  
*... and the necessary ecosystem*



# What's new



## noel3



# Why do we develop these things?

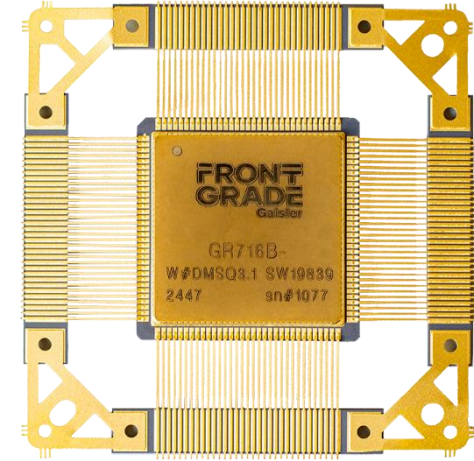
"We do these things not because they are easy,

# Why do we develop these things?

"We do these things not because they are easy,  
but because we thought they were going to be easy"

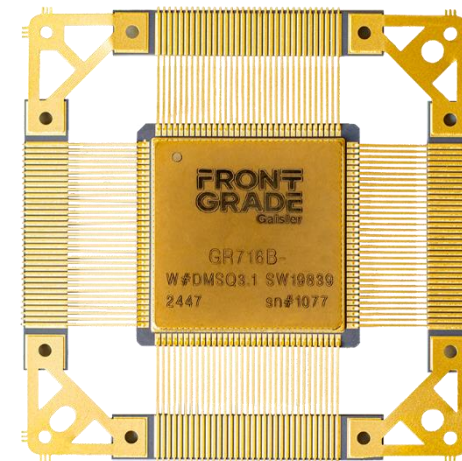
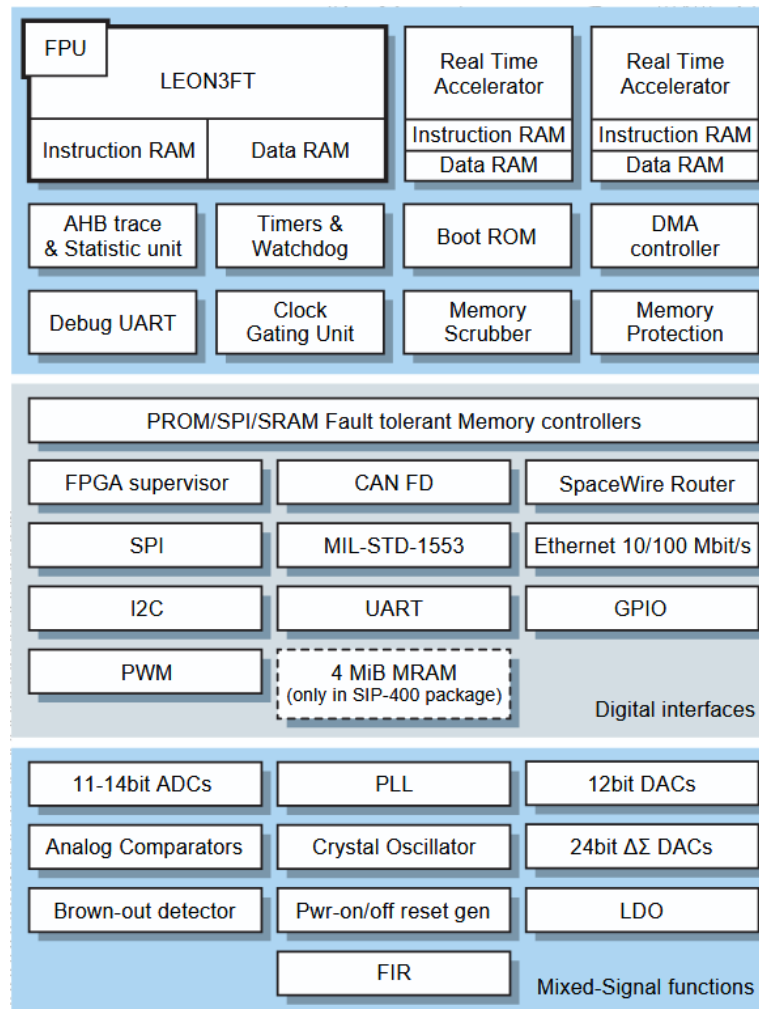
- The Programmers' Credo

# Why GR716B?

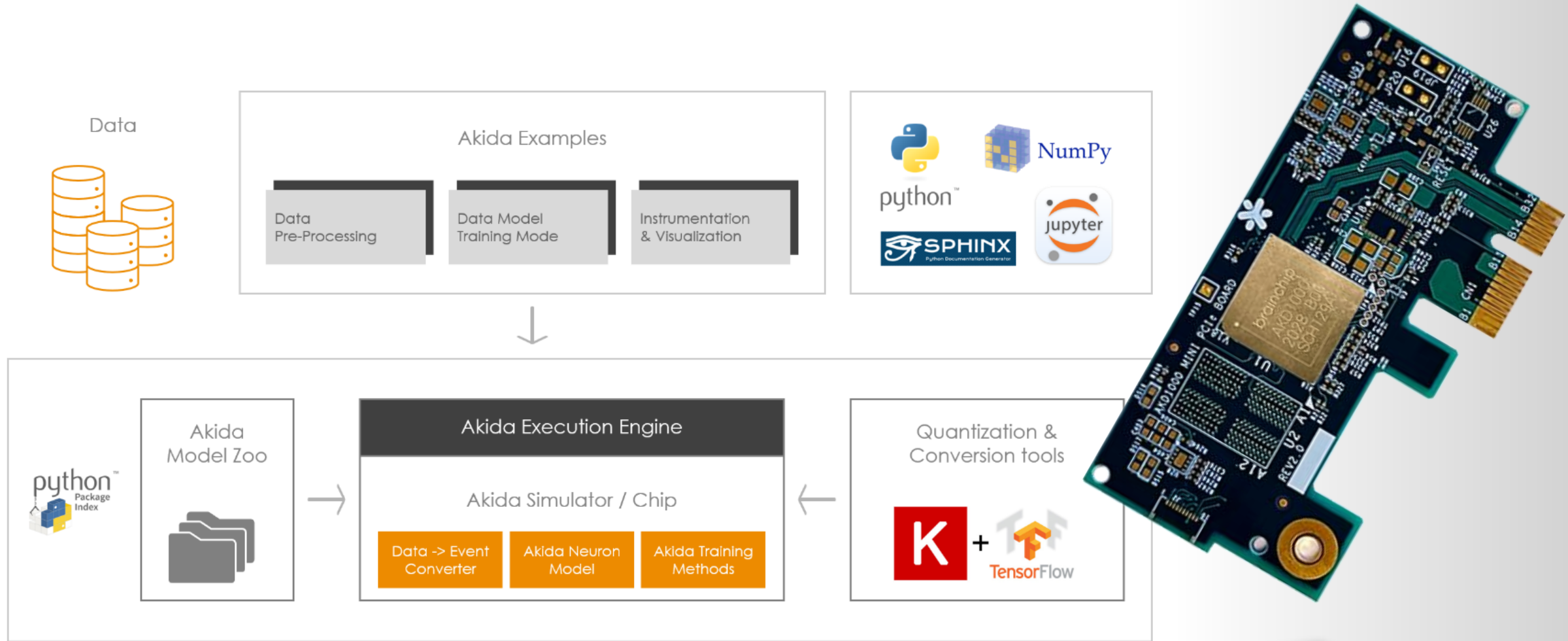


# Why GR716B?

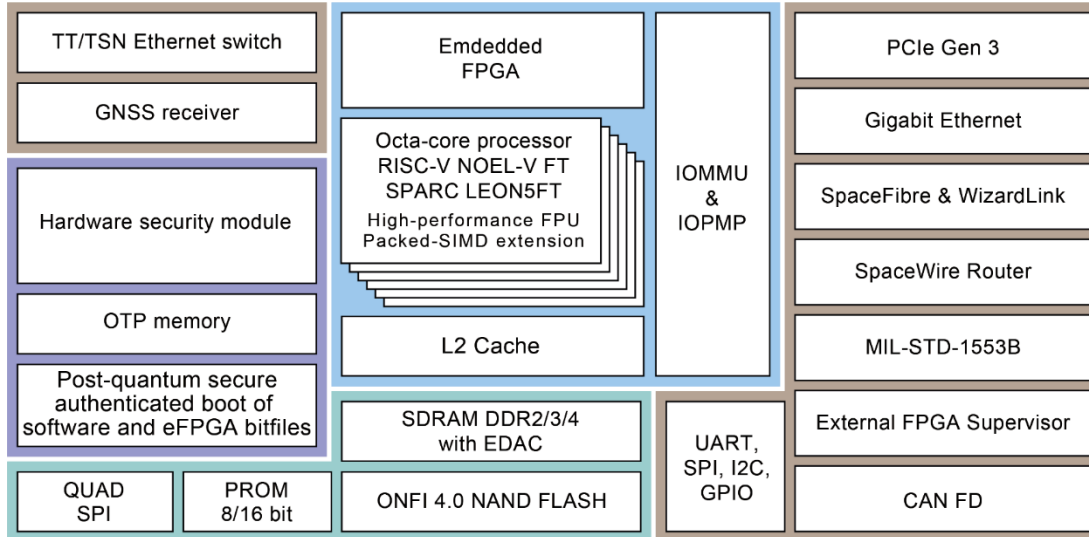
- Single 3.3V supply possible (CQFP, PBGA)
- Many digital interfaces (including Ethernet)
- On-chip Oscillator, BO, POR
- Simultaneous sampling of ADC channels
- AMD FPGA programming and Scrubbing
- Real time software execution:
  - deterministic instruction execution time
  - fixed interrupt latency
- Capability to sense core voltage for trimming of the embedded voltage regulator for low power applications
- Fault tolerant – less than 1E-5 event/device/day in typical LEO and GEO orbits



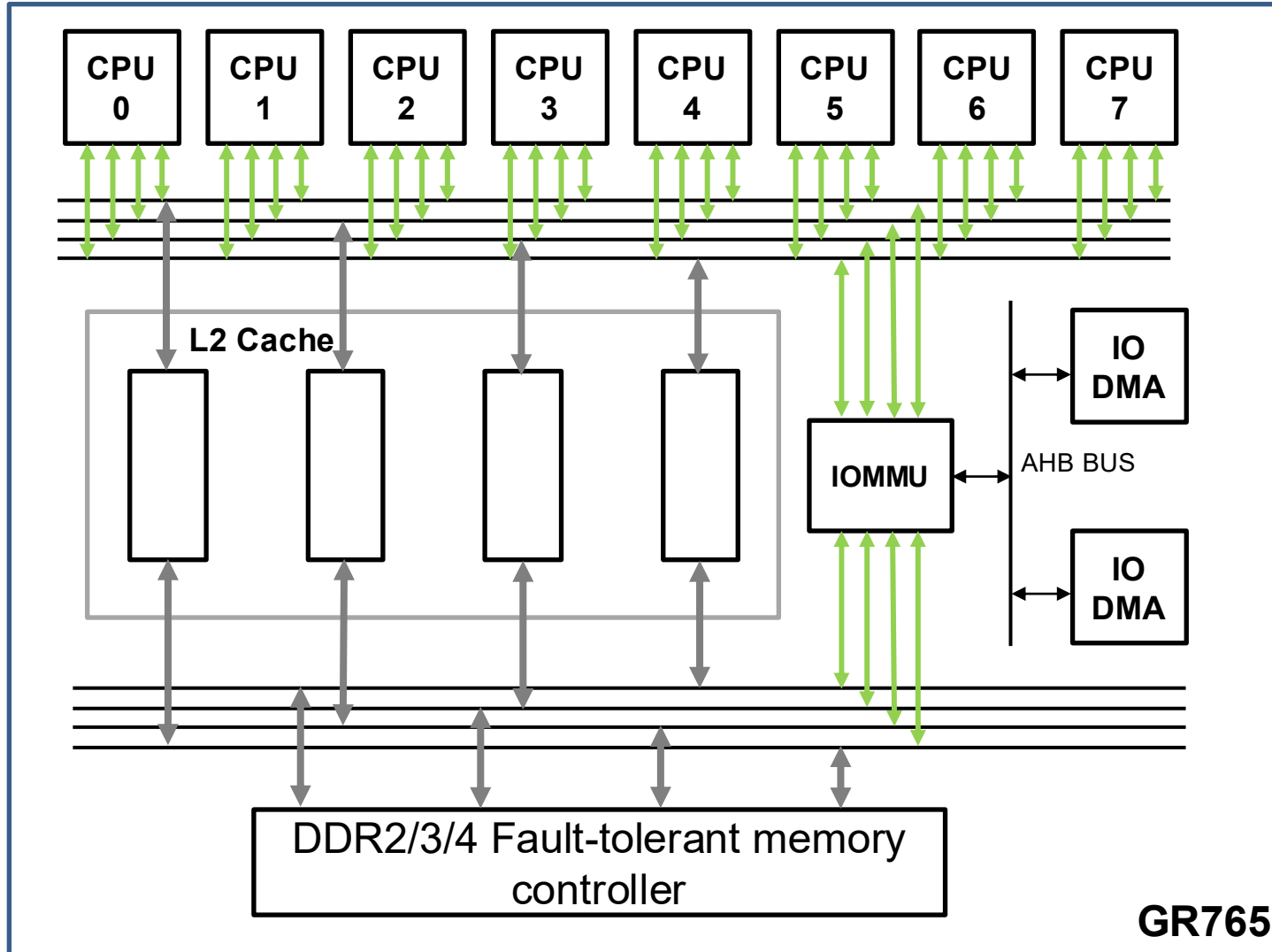
# Why GR801?



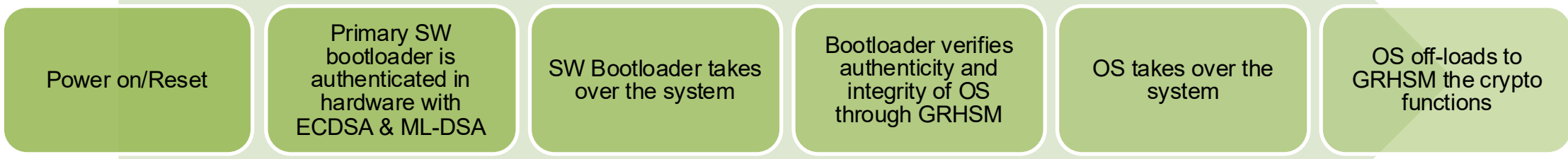
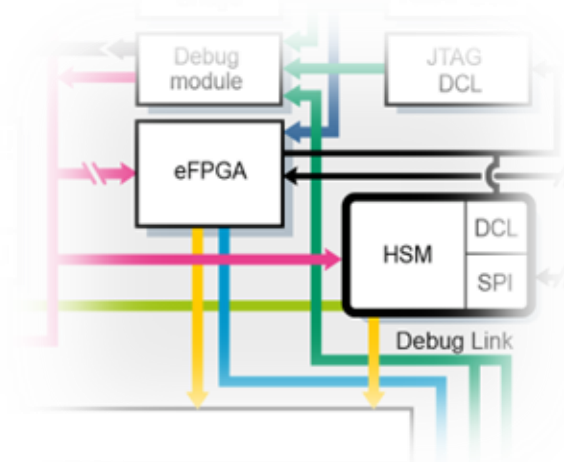
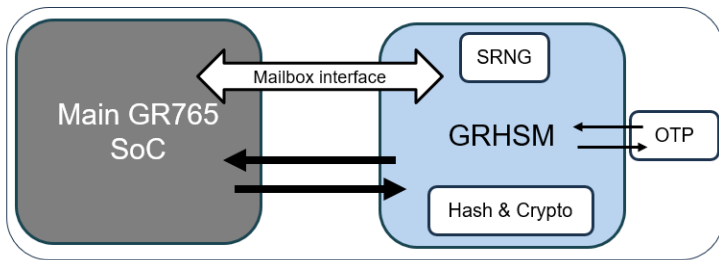
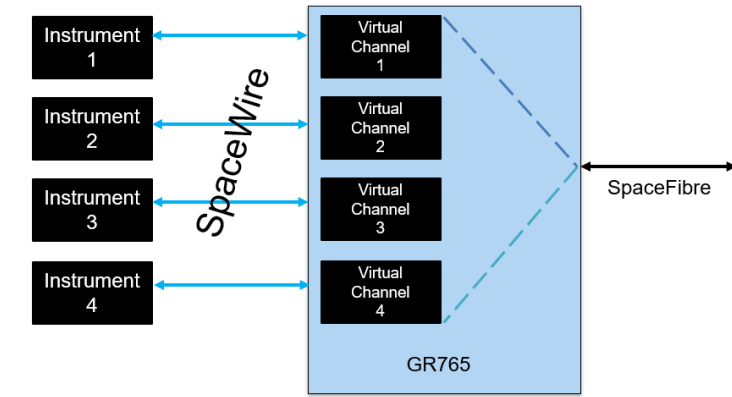
# Why GR765?



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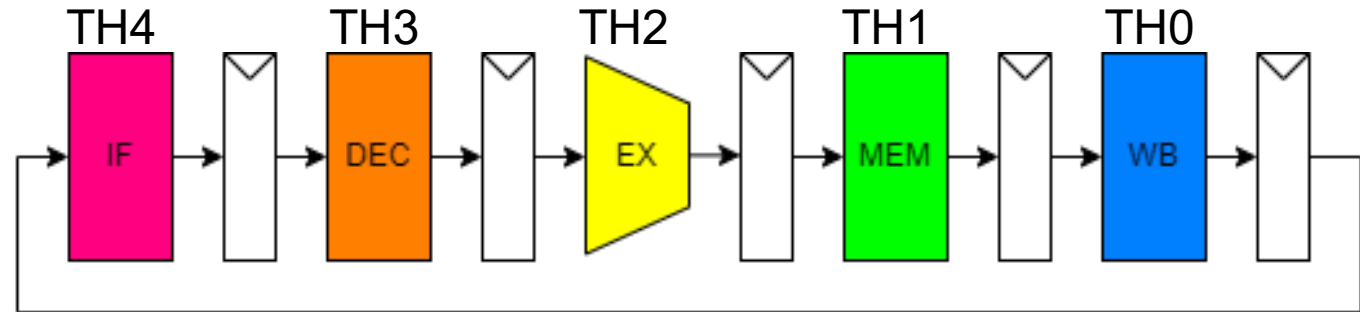


Metric	GR740	GR765	Change
CPU performance	4-core, single-issue, 250MHz	8-core, dual-issue, 800 MHz	<b>12x</b>
RAM capacity	SDRAM PC100, 512 MiB	DDR4-1600, 16 GiB	<b>32x</b>
RAM bandwidth	64 x 100Mbps = 6.4 Gbps	64 x 1600 Mbps = 100 Gbps	<b>16x</b>
IO bandwidth (in+out)	PCI 32x33M = 1Gbps SpW 8x2x200M = 3.2 Gbps	PCIe 8x2x4G = 64 Gbps SpFi 4x2x6.25 = 50 Gbps	<b>27x</b>

# Why NOEL3?

## Barrel architecture?

- Fine-grained multithreading processor
- Only one instruction per thread is executed in the pipeline at the same time
- Number of stages = Number of threads



## Why barrel architecture?

- Small area
  - No data dependencies/forwarding, no branch prediction, no speculation
- Easier verification
  - Mostly 1-iteration instructions
  - In-order pipeline, instruction retires before next one starts
- High multithreading performance

Cycle	Thread retiring instruction
0	Thread 0
1	Thread 1
2	Thread 2
3	Thread 3
4	Thread 4
5	Thread 0
6	Thread 1
7	Thread 2
8	Thread 3
9	Thread 4

# Trends

- Shorter lifetime of platforms
- Shorter development cycles
- Rapid LEO expansion
- Space-specific standards don't fly anymore
- Acceptance of commercial technology and development flow – “Does it run Linux?”
- Cybersecurity awareness and requirements
- Non-dependence
- Monolithic chip vs chiplets



Funded by  
the European Union

# ePERFECT

European High-Performance Processor  
for RF Defense Applications



**FRONTGRADE**  
Gaisler

Frontgrade Gaisler is proud to support the European Union and the European Defence Fund with our fault-tolerant RISC-V microprocessor technology for the creation of European semiconductor supply and value chains.

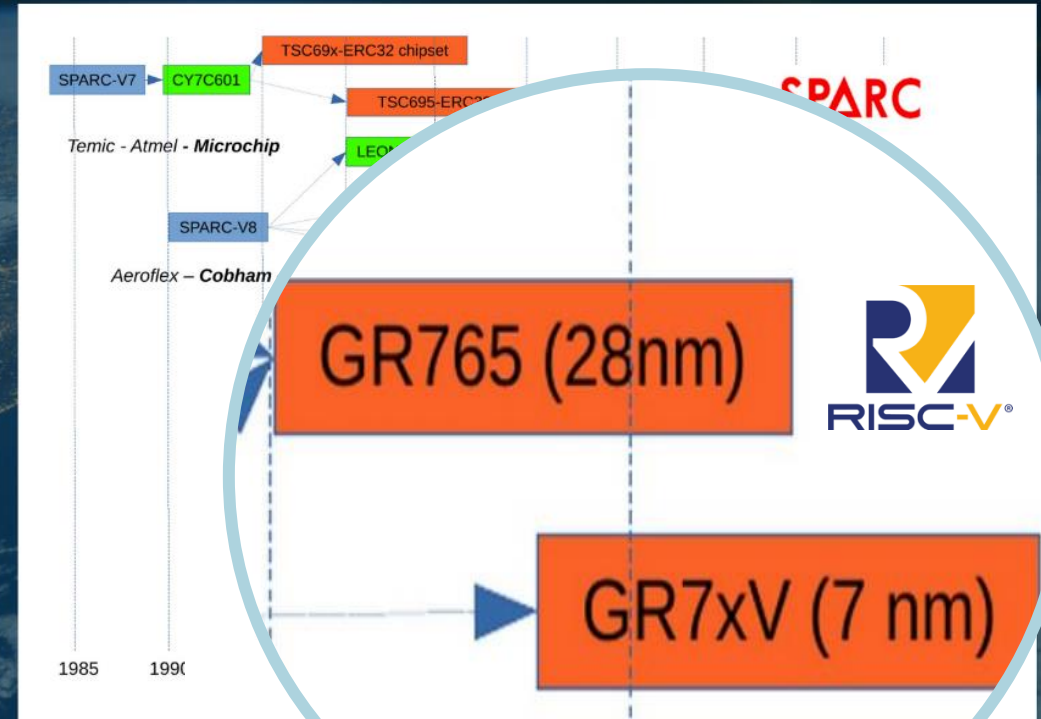
## 2021/22: RISC-V@ESA in Fast Forward Mode

- Concept study for GR7xV HPC started in ARTES in 2021
- Target 7 nm – technology not available for space
- 2022 started with a “shoestring” ITT in TDE: 450k€
- Can we do RISC-V prototypes in 22-28 nm technology?
- Synergy with GR765 (originally planned as 8-core LEON5 only)
- → RISC-V is **hitch-hiking** on SPARC, saving cost...
- Only CPU cores are duplicated, but cache RAM and SoC shared
- **Facilitates transition for users: one chip, one board, two modes**
- GR765 phase 2 released with ARTES funding also in 2022
- Today ~ 4 M€ public funding committed into GR765 / GR7xV
- complemented by significant co-funding
- Prototypes funded, flight parts (ROM cost 4.5 M€) TBC



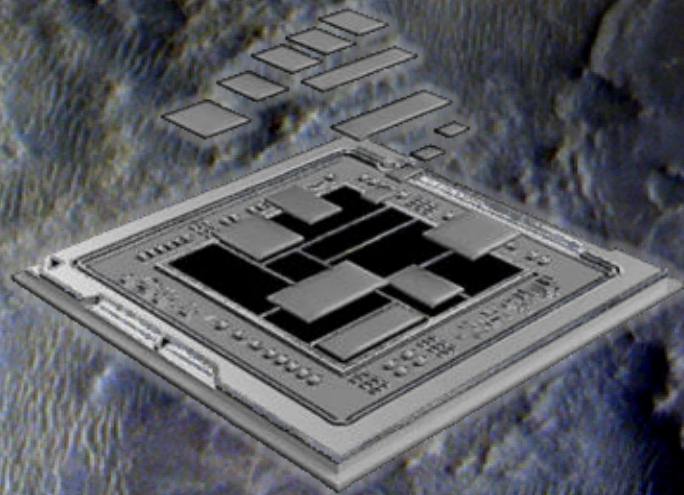
## Space Micropocessor Roadmaps in Europe

- Almost 30 years of SPARC
- LEON chips by Microchip and Cobham Gaisler (CG)
- CG transition to RISC-V
- RISC-V on Microchip PolarFire-SoC FPGA
- NASA HPSC-new opted RISC-V (SiFive/Microchip)
- NX roadmap: ARM
- ARM also on Xilinx FPGA



# GR7xV – European 16-core space processor on 7nm

**RISC-V**



Ultra Deep Sub-Micron

