

The Thales logo is displayed in a bold, white, sans-serif font. The letter 'A' is stylized with a dot in the center. The background behind the logo consists of several overlapping, semi-transparent blue circles of varying shades, creating a layered effect.

THALES

Building a future we can all trust

A white horizontal line with a slight 3D effect, appearing as if it's floating above the surface, extending from the left edge of the slide towards the center.

Thales and RISC-V a tale of hardware sovereignty

Daniel Glazman

CTO Software – Thales Group

Thales key figures



83,000
employees



68 countries
A global footprint



More than **€4 bn***
* including €1,1 bn
in self-funded R&D



€20.6 bn
revenues



Thales group Overview

Space

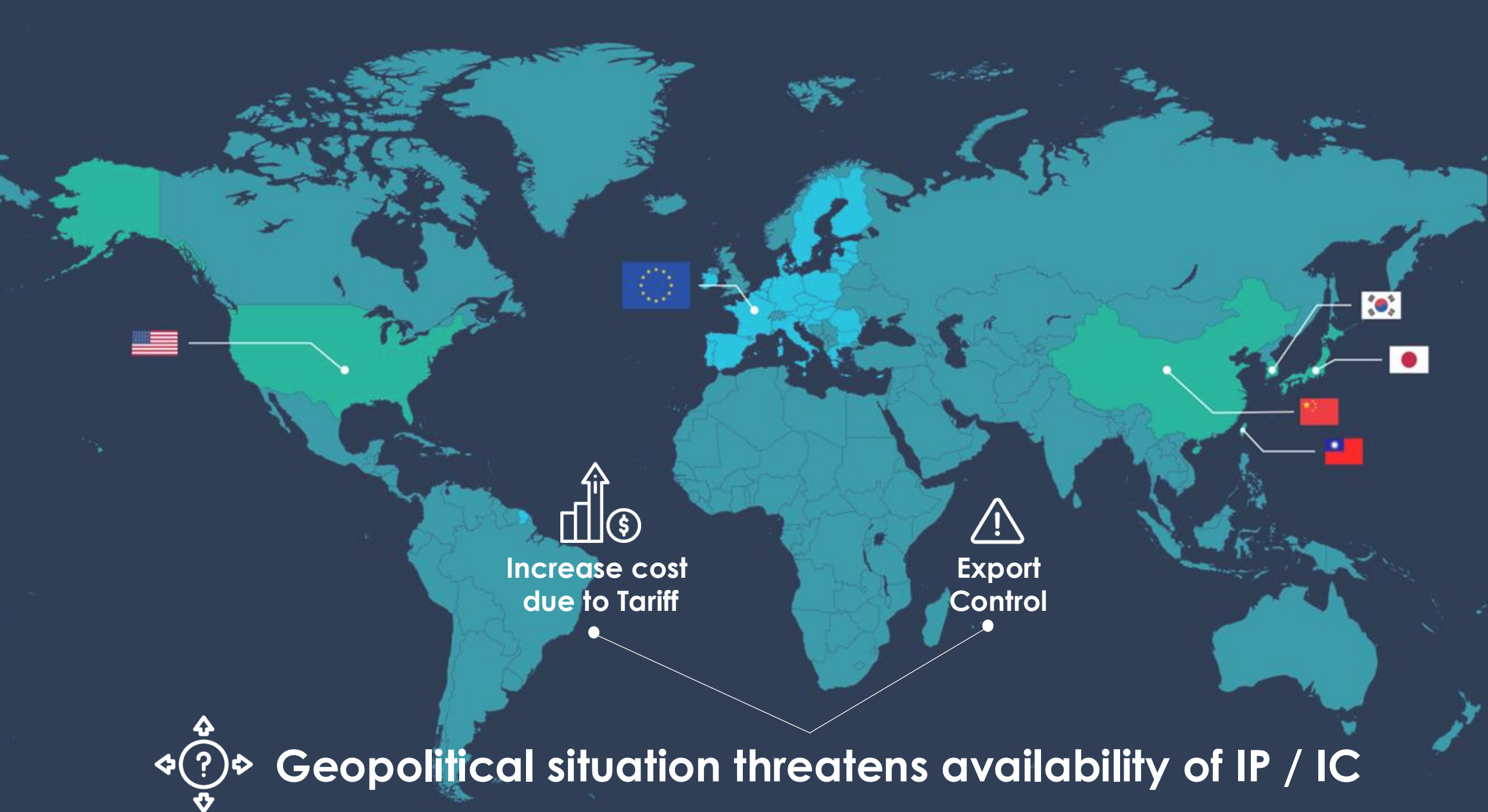
Avionics

Defense

Communication

Cyber Security





Increase cost
due to Tariff



Export
Control



Geopolitical situation threatens availability of IP / IC

Digital Sovereignty



**Safe
Secure**



**Open Source HW
Open Source SW**



Independent

Why Thales invests in RISC-V and Open Source HW?

Share cost instead of purchasing IP

Open-source community

Sovereignty

*Possible commercial exploitation without export constraints
Enable strong EU investment*

Safety

No black-box

SWaP & customization

Exact fit between features and application needs

Security

A fully auditable processor

No vendor-locking

Business opportunities for support, customization...

Software

Large ecosystem compatible across implementations

Performance

State-of-the-art processor



Thales member of the **OpenHW Foundation (Eclipse)** and **RISC-V International**

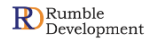
Thales Innovation

Open Source Industrial Grade CVA6 μ Controller

- ▶ **CV32A60X**: Low area and High performance CVA6 Core
- ▶ 100% Verified
- ▶ Sovereign
- ▶ Available for integration into silicon products (TRL5) w/o royalties!



Contributors to CVA6 OpenHW ecosystem



What matters to us in the CVA6 SW ecosystem

Boot and
FW

- **U-Boot**
- **OpenSBI**

OS/hyp.
support

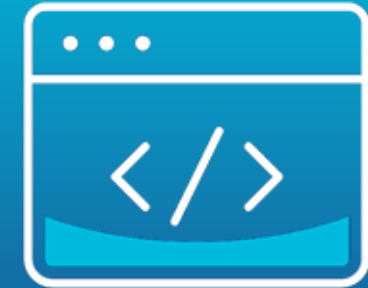
- **RTEMS**
- **PikeOS** (WIP)
- **Linux**: 32 & 64 bit
- **Yocto**, **Buildroot**
- **FreeRTOS**, **Zephyr**
- **BAO** hypervisor (CV64A6 only)

Compiler

- Standard **GCC**
- Libraries: **glibc**, Newlib ...
- CLANG/LLVM, **RUST**

Debug

- HW and baremetal: JTAG probe, OpenOCD, **GDB**/Eclipse IDE, VSCode
- Linux-based: GDB server



Full open-source software
ecosystem

Protect your HW investments

RISC-V student contest

> Organized by



> Objectives

- ▶ Promote RISC-V and computer architecture in French education
- ▶ Extend RISC-V and OpenHW communities
- ▶ Strengthen industry-academy connections

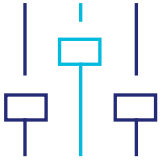
> Past years

- ▶ 2020-2021: Improve CV32A6 FPGA performance
 - 13 teams from 10 universities / awarded: Télécom Paris, U. Toulouse III
- ▶ 2021-2022: Improve CV32A6 energy efficiency
 - 12 teams from 7 universities / awarded: U. Strasbourg (2 teams), IMT Atlantique
- ▶ 2022-2023: Focus on CV32A6 cybersecurity
 - 19 teams from 14 universities / awarded: INSA Toulouse, CentraleSupélec
- ▶ 2023-2024: AI acceleration in CV32A6
 - 13 teams from 11 universities / awarded: IMT Atlantique (2 teams)
- ▶ 2024-2025: increase CV32A6 frequency
 - 12 teams from 10 universities
 - Awarded: Mines Saint-Étienne, Université de Rennes ISTIC



Student Annual contests

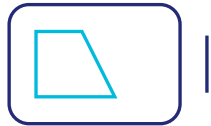
2020-2021



Optimize CVA6 performance and surface

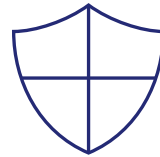
13 Teams

2021-2022



Optimize CVA6 energy efficiency

2022-2023



Defeat cyber-attacks against CVA6 running Zephyr OS

2023-2024



Accelerate MNIST digit recognition with extensions of CVA6

2024-2025



Increase CVA6 frequency on FPGA

2025-2026 kicked off: FFT acceleration on CV32A6

Acknowledgements



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Thank you

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